CLAIMS

1. A process for applying a metallization interconnect structure to a semiconductor workpiece, the workpiece including a barrier layer deposited on a surface thereof, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the barrier layer, the seed layer having a thickness of less than or equal to about 500 Angstroms;

(b) enhancing the ultra-thin seed layer by depositing additional metal to provide an enhanced seed layer, the enhanced seed layer having a thickness at all points on sidewalls of substantially all recessed features distributed within the workpiece that is equal to or greater than about 10% of the nominal seed layer thickness over an exteriorly disposed surface of the workpiece.

2. The process of claim 1 wherein the additional metal is copper.

3. The process of claim 1 wherein the ultra-thin seed layer is enhanced by a process comprising an electrochemical deposition step.

4. The process of claim 3 wherein the electrochemical deposition step occurs in an alkaline bath.

5. The process of claim 4 wherein the alkaline bath comprises metal ions and an agent effective in complexing the metal ions.

6. The process of claim 1 wherein the ultra-thin metal seed layer formed in step (a) is formed by physical vapor deposition.

7. The process of claim 1 wherein the ultra-thin metal seed layer formed in step (a) has a thickness of about 50 to about 500 Angstroms.

8. The process of claim 7 wherein the ultra-thin metal layer formed in step (a) has a thickness of about 100 to about 250 Angstroms.

9. The process of claim 1 wherein the complexing agent is comprised of one or more complexing agents selected from EDTA, ED, and polycarboxylic acid.

10. The process of claim 5 wherein the complexing agent is comprised of EDTA and the EDTA in the bath has a concentration within the range of 0.03 to 1.0 M.

11. The process of claim 9 wherein the complexing agent is comprised of ED and wherein the ED in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

12. The process of claim 10 wherein the complexing agent is comprised of EDTA and the EDTA has a concentration within the range of 0.1 to 0.4 M.

13. The process of claim 9 wherein the complexing agent is comprised of citric acid and the citric acid in the bath has a concentration within the range of 0.03 to 1.0 M.

14. The process of claim 4 and further comprising the step of subjecting the semiconductor workpiece to a further electrochemical deposition process in an acidic electrolytic solution to complete deposition of the metal to a thickness needed for the formation of the interconnect structure.

15. The process of claim 14 and further comprising the step of subjecting the semiconductor workpiece to a rinsing process after electrochemical deposition in the outline bath and prior to the further electrochemical copper deposition process in an acidic electrolytic solution.

16. In a manufacturing line including a plurality of apparatus for the manufacture of integrated circuits, one or more apparatus of the plurality of apparatus being used for applying a copper metallization interconnect

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structure to a surface of a semiconductor workpiece used to form the integrated circuits, the one or more apparatus comprising:

means for applying a conductive ultra-thin seed layer to a surface of the semiconductor workpiece;

means for electrochemically enhancing the conductive ultra-thin seed layer to render it suitable for subsequent electrochemical application of the copper interconnect metallization to a predetermined thickness representing a bulk portion of the copper interconnect metallization structure.

17. One or more apparatus as claimed in claim 16 wherein the means for applying is further defined by means for applying a conductive ultra-thin copper seed layer to a barrier layer surface of the ~~semiconductor~~ microelectronic workpiece.

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~~18~~. One or more apparatus as claimed in claim 16 wherein the means for applying is further defined by means for applying a conductive ultra-thin copper seed layer to a barrier layer surface of the ~~semiconductor~~ microelectronic workpiece using a PVD process.

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~~19~~. One or more apparatus as claimed in claim 16 wherein the means for applying is further defined by means for applying a conductive ultra-thin

copper seed layer to a barrier layer surface of the ~~semiconductor~~ microelectronic workpiece using a CVD process.

20. One or more apparatus as claimed in claim 17 wherein the means for electrochemically enhancing the conductive ultra-thin seed layer is further defined by means for electrochemically enhancing the conductive ultra-thin seed layer by electrochemically depositing copper using an alkaline copper bath having a complexing agent.

21. One or more apparatus as claimed in claim 20 wherein the electrochemical enhancement of the ultra-thin seed layer takes place at a plating voltage having a magnitude that is at least about or greater than 1.1 volts.

22. One or more apparatus as claimed in claim 20 wherein the alkaline bath has a pH > or equal to about 9.0.

23. One or more apparatus as claimed in claim 20 wherein the complexing agent is comprised of EDTA.

24. One or more apparatus as claimed in claim 20 wherein the complexing agent is comprised of ED.

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~~25~~. One or more apparatus as claimed in claim ~~20~~ wherein the complexing agent is a comprised of a carboxylic acid or salt thereof.

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~~26~~. One or more apparatus as claimed in claim ~~25~~ wherein the complexing agent is citric acid or salt thereof.

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27. One or more apparatus as claimed in claim 20 and further comprising means for electrochemically adding a further layer of copper over the conductive ultra-thin seed layer by electrochemically depositing copper using an acidic copper bath.

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~~28~~. One or more apparatus as claimed in claim ~~27~~ wherein the electrochemical enhancement of the ultra-thin seed layer takes place at a plating voltage having a magnitude that is greater than the magnitude of the plating voltage in the acidic copper bath.

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~~29~~. One or more apparatus as claimed in claim ~~28~~ and further comprising means for rinsing the ~~semiconductor~~ microelectronic workpiece prior to its introduction to the means for electrochemically adding a further layer of copper.

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30. A process for applying a metallization interconnect structure to a semiconductor workpiece, the workpiece including a barrier layer deposited on a surface thereof, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the barrier layer, the seed layer having a thickness of less than or equal to about 500 Angstroms;

(b) subjecting the semiconductor workpiece to an electrochemical copper deposition process in an alkaline electrolytic bath having copper ions complexed with a complexing agent such that additional copper is deposited on the ultra-thin copper seed layer to thereby enhance the seed layer.

31. The process of claim 30 wherein the ultra-thin metal seed layer formed in step (a) is formed by physical vapor deposition.

32. The process of claim 30 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 50 to about 500 Angstroms.

33. The process of claim 32 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 100 to about 250 Angstroms.

34. The process of claim 33 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 200 Angstroms.

35. The process of claim 30 wherein the alkaline electrolytic bath has a pH of at least 9.0.

36. The process of claim 30 wherein the copper ions in the electrolytic bath are provided by copper sulfate.

37. The process of claim 36 wherein the copper sulfate in the electrolytic bath has a concentration within the range of 0.03 to 0.25 M.

38. The process of claim 36 wherein the concentration of copper sulfate is about 0.1 M.

39. The process of claim 30 wherein the copper complexing agent is comprised of a copper complexing agent selected from EDTA, ED, and citric acid.

40. The process of claim 39 wherein the complexing agent is comprised of EDTA and the EDTA in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

41. The process of claim 39 wherein the complexing agent is comprised of ED and the ED in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

42. The process of claim 39 wherein the complexing agent is comprised of EDTA and the EDTA has a concentration within the range of 0.1 to 0.4 M.

43. The process of claim 39 wherein the complexing agent is comprised of citric acid and the citric acid in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

44. The process of claim 43 wherein the citric acid has a concentration within the range of 0.1 to 0.4 M.

45. The process of claim 30 and further comprising the step of subjecting the semiconductor workpiece to a further electrochemical copper deposition process in an acidic electrolytic solution to complete deposition of the copper to a thickness needed for the formation of the copper interconnect structure.

46. The process of claim 45 and further comprising the step of subjecting the semiconductor workpiece to a rinsing process after step (b) and prior to the further electrochemical copper deposition process in an acidic electrolytic solution.

~~47. A semiconductor workpiece~~ comprising:

a plurality of the recessed structures distributed in a face of the semiconductor workpiece;

an enhanced seed layer having a thickness at all points on sidewalls of substantially all recessed features distributed within the workpiece that is equal to or greater than about 10% of the nominal seed layer thickness over an exteriorly disposed surface of the workpiece.

48. A semiconductor workpiece as claimed in claim 48 wherein the thickness of the sidewalls of substantially all recessed features is equal to or greater than about ~~20%~~.

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